Abstracts

Spiral inductor performance in deep-submicron bulk-CMOS with copper interconnects (2002 [RFIC])

W.B. Kuhn, A.W. Orsborn, M.C. Peterson, S.R. Kythakyapuzha, A.I. Hussein, Jun Zhang, Jianming Li, E.A. Shumaker and N.C. Nair. "Spiral inductor performance in deep-submicron bulk-CMOS with copper interconnects (2002 [RFIC])." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 385-388.

This paper reviews design considerations for spiral inductors in bulk CMOS and reports investigations carried out in a commercial 0.18 /spl mu/m process using 6-layer copper metallization. Quality factors of approximately 8 are measured for 10 nH spirals operating between 1 and 2 GHz. Comparisons of Q and self-resonant frequency are provided for a variety of construction variables including with/without a patterned ground shield, metal-6 only versus stacking layers 3 thru 6, dense versus sparse vias, wide versus narrow traces, and with/without metal-fill.

❑ Return to main document.